

- (b) etching the first portion of a first of said plurality of wiring lines, such that the first portion has a planar surface completely across said first portion, joining said side walls, and is thinner in height relative to said surface of said core layer than the second portion, such that cross-talk noise between adjacent two wiring lines is reduced, wherein the first portion is parallel to at least one of the plurality of wiring lines other than the first of the plurality of wiring lines.

Claim 38. The method as claimed in claim 37, wherein a second of said plurality of said wiring lines is provided, spaced from said first wiring line of said plurality of wiring lines having said first and second portions, said second wiring line having third and fourth portions, and etching said second wiring line such that the third portion is thinner in height relative to said surface of said core layer than the fourth portion, wherein the third portion is parallel to the first portion.

In the Office Action dated March 3, 2006, Claims 37 and 38 were rejected as anticipated under 35 U.S.C. 102(b) by Gali et al. ( U.S. 3,781,596). The Office Action alleges that Gali discloses etching of (71) to form a plurality of wiring lines on a surface of a core layer and further etching (71) using a mask to form a different thickness first portion (12) then a second portion (13), referring to Fig. 1a. Fig. 2 is referred to to show a first portion of one line with (13) parallel with another line (12) other than the one next to (13). Reconsideration and removal of this rejection is respectfully requested in view of the following remarks.

The purpose of applicant's method is to form a plurality of wiring lines on a board in a manner that reduces cross-talk noise between adjacent two wiring lines.

The Gali reference makes no reference whatsoever to cross-talk or how to reduce the same. This is because the length of Gali's wiring line is only a few millimeters. As stated at Col. 1, lines 19-21 of Gali et al.; "This invention relates to semiconductor chips, and more specifically, to mounting such chips on substrates." Thus, it is readily apparent that the size of the wiring lines would be in the range of only a few millimeters. With such a short length, cross-talk would not be an issue. In the present method, however, with reference to Fig. 1 of the present specification, by comparing the size of semiconductors 2a, 2b, and 2c with wiring lines among them, portions of the wiring lines in the present invention are longer than the widths of the semiconductors 2a, 2b, and 2c. Accordingly, it is obvious that the length of the wiring lines of the present invention are longer than the length of the wiring lines of Gali and can be recognized to be dozens of millimeters.

As previously mentioned, Gali does not disclose anywhere a problem of cross-talk noise, and this is because his etched portions would be only a few millimeters in length and have a uniform height except for pads (13).

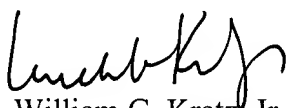
The disclosure of the Gali et al. reference simply does not lead one to the present claimed method of forming a plurality of wiring lines on a board such that cross-talk between adjacent two wiring lines is reduced, and only the teachings of Applicant's specification would lead one to the present method.

U.S. Patent Application Serial No. **09/928,441**  
Amendment dated April 24, 2007

If there are any issues of a minor nature remaining, the Examiner is urged to contact Applicant's attorney, the undersigned, at Area Code (202) 659-2930.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP



William G. Kratz, Jr.  
Attorney for Applicant  
Reg. No. 22,631

WGK/jls

Atty. Docket No. **000958A**  
Suite 1000, 1725 K Street, N.W.  
Washington, D.C. 20006  
(202) 659-2930



**23850**

PATENT TRADEMARK OFFICE

Q:\FLOATERS\WGK\00\000958A\prelim remarks 04-23-07